CLAIMS

What is claimed is:

1. An integrated circuit device having an ultra-low power timer, comprising:

a voltage comparison and logic module having an input, an output and a first enable,

wherein a predetermined current value is drawn at the input when the voltage comparison and logic module is enabled,

the output is at a first logic level when a voltage on the input is less than or equal to a reference voltage, and

the output is at a second logic level when the voltage on the input is greater than the reference voltage;

an external connection of an integrated circuit device, wherein the external connection is coupled to a digital output of the integrated circuit device and to the input of the voltage comparison and logic module; and

a timing capacitor coupled to the external connection, whereby the digital output of the integrated circuit device charges the timing capacitor and the input of the voltage comparison and logic module discharges the timing capacitor.

2. The integrated circuit device of claim 1, wherein the voltage comparison and logic module comprises:

a voltage comparator having a first input coupled to the input of the voltage comparison and logic module, and a second input coupled to the reference voltage; and

a logic circuit coupled to the voltage comparator, the output of the voltage comparison and logic module and the first enable.

3. The integrated circuit device of claim 2, further comprising a low current source having an enable, the low current source is coupled to the input of the voltage comparison and logic module, wherein the low current source enable activates the low current source to draw current from the external connection.

4. The integrated circuit device of claim 1, wherein the digital output comprises series connected first and second transistors, wherein the first transistor couples a first voltage to the external connection and the second transistor couples a second voltage to the external connection.

5. The integrated circuit device of claim 4, wherein the first transistor charges the timing capacitor to the first voltage.

6. The integrated circuit device of claim 4, wherein the second transistor discharges the timing capacitor to the second voltage.

7. The integrated circuit device of claim 1, further comprising a first external resistor connected in parallel with the timing capacitor.

8. The integrated circuit device of claim 1, further comprising a second external resistor connected in series with the timing capacitor.

9. The integrated circuit device of claim 1, wherein the first logic level causes the integrated circuit device to wake-up when in a sleep mode.

10. An integrated circuit device having an ultra-low power programmable timer, comprising:

a voltage comparison and logic module having an input, an output and a first enable,

wherein a predetermined current value is drawn at the input when the voltage comparison and logic module is enabled,

the output is at a first logic level when a voltage on the input is less than or equal to a reference voltage, and

the output is at a second logic level when the voltage on the input is greater than the reference voltage;

an external connection of an integrated circuit device, wherein the external connection is coupled to a digital output of the integrated circuit device and to the input of the voltage comparison and logic module; and

a timing circuit coupled to the external connection, whereby the digital output of the integrated circuit device discharges the timing circuit and charges

the timing circuit to a predetermined voltage value, and the input of the voltage comparison and logic module discharges the timing circuit.

11. The integrated circuit device of claim 10, wherein the voltage comparison and logic module comprises:

a voltage comparator having a first input coupled to the input of the voltage comparison and logic module, and a second input coupled to the reference voltage; and

a logic circuit coupled to the voltage comparator, the output of the voltage comparison and logic module and the first enable.

12. The integrated circuit device of claim 11, further comprising a low current source having an enable, the low current source is coupled to the input of the voltage comparison and logic module, wherein the low current source enable activates the low current source to draw current from the external connection.

13. The integrated circuit device of claim 10, wherein the digital output comprises series connected first and second transistors, wherein the first transistor couples a first voltage to the external connection and the second transistor couples a second voltage to the external connection.

14. The integrated circuit device of claim 13, wherein the second transistor discharges the timing circuit to the second voltage.

15. The integrated circuit device of claim 13, wherein the first transistor charges the timing circuit to the predetermined voltage.

16. The integrated circuit device of claim 10, wherein the timing circuit comprises a timing capacitor and first resistor, wherein the timing capacitor and the first resistor are connected in parallel.

17. The integrated circuit device of claim 16, wherein the timing circuit further comprises a second resistor connected in series with the timing capacitor.

18. The integrated circuit device of claim 10, wherein the first logic level causes the integrated circuit device to wake-up when in a sleep mode.

19. An integrated circuit device having a programmable low-voltage detection (PLVD) circuit, comprising:

a voltage comparison and logic module having an input, an output and a first enable,

wherein a predetermined current value is drawn at the input when the voltage comparison and logic module is enabled,

the output is at a first logic level when a voltage on the input is less than or equal to a reference voltage, and

the output is at a second logic level when the voltage on the input is greater than the reference voltage;

an external connection of an integrated circuit device, wherein the external connection is coupled to a digital output of the integrated circuit device and to the input of the voltage comparison and logic module; and

a timing capacitor coupled to the external connection, whereby the digital output of the integrated circuit device charges the timing capacitor and the input of the voltage comparison and logic module discharges the timing capacitor.

20. The integrated circuit device of claim 19, wherein the voltage comparison and logic module comprises:

a voltage comparator having a first input coupled to the input of the voltage comparison and logic module, and a second input coupled to the reference voltage; and

a logic circuit coupled to the voltage comparator, the output of the voltage comparison and logic module and the first enable.

21. The integrated circuit device of claim 20, further comprising a low current source having an second enable, the low current source is coupled to the input of the voltage comparison and logic module, wherein the second enable activates the low current source to draw current from the external connection.

22. The integrated circuit device of claim 19, wherein the digital output comprises series connected first and second transistors, wherein the first transistor couples a first voltage to the external connection and the second transistor couples a second voltage to the external connection.

23. The integrated circuit device of claim 22, wherein the first transistor charges the timing capacitor to the first voltage.

24. The integrated circuit device of claim 22, wherein the second transistor discharges the timing capacitor to the second voltage.

25. The integrated circuit device of claim 19, further comprising a first external resistor connected in parallel with the timing capacitor.

26. The integrated circuit device of claim 19, wherein the first logic level indicates a low battery voltage condition and the second logic level indicates a desired battery condition.

27. The integrated circuit device of claim 19, wherein the first logic level indicates a low voltage condition.

28. The integrated circuit device of claim 27, wherein if the first logic level occurs within a certain time period there is a low voltage condition.

29. A method of timing with an ultra-low power timer in an integrated circuit device, said method comprising the steps of:

charging a timing capacitor to a first voltage with an output of an integrated circuit device;

discharging the timing capacitor with a predetermined current value;

comparing the discharging timing capacitor voltage with a reference voltage;

outputting a first logic level when the discharging timing capacitor voltage is greater than the reference voltage, and

outputting a second logic level when the discharging timing capacitor voltage is less than or equal to the reference voltage.

30. A method of timing with an ultra-low power programmable timer in an integrated circuit device, said method comprising the steps of:

discharging a timing capacitor to a second voltage with an output of an integrated circuit device;

charging the timing capacitor to a first voltage with the output of the integrated circuit device within a first time;

discharging the timing capacitor with a predetermined current value;

comparing the discharging timing capacitor voltage with a reference voltage;

outputting a first logic level when the discharging timing capacitor voltage is greater than the reference voltage, and

outputting a second logic level when the discharging timing capacitor voltage is less than or equal to the reference voltage.

31. A method of detecting low battery voltage with a programmable low voltage detector (PLVD) in an integrated circuit device, said method comprising the steps of:

charging a timing capacitor to a first voltage with an output of an integrated circuit device at certain time intervals;

discharging the timing capacitor with a predetermined current value;

comparing the discharging timing capacitor voltage with a reference voltage;

outputting a first logic level when the discharging timing capacitor voltage is greater than the reference voltage, and

outputting a second logic level when the discharging timing capacitor voltage is less than or equal to the reference voltage.

32. A method of detecting low battery voltage with a programmable low voltage detector (PLVD) in an integrated circuit device, said method comprising the steps of:

charging a timing capacitor to a first voltage with an output of an integrated circuit device;

discharging the timing capacitor with a predetermined current value;

comparing the discharging timing capacitor voltage with a reference voltage within a certain time period;

outputting a first logic level when the discharging timing capacitor voltage is greater than the reference voltage, and

outputting a second logic level when the discharging timing capacitor voltage is less than or equal to the reference voltage within the certain time period.

33. A method of determining temperature with a low-voltage detection circuit, said method comprising:

determining a trip voltage value with an integrated circuit voltage comparator; and

calculating a temperature from a know temperature by determining a difference between the trip voltage value and a known voltage value, then dividing the difference by a constant.

34. The method of claim 33, wherein the known voltage value, the know temperature and the constant are stored in a memory.

35. A method of determining temperature with a low-current source, said method comprising:

determining a current value of a low-current source; and

calculating a temperature from a know temperature by determining a difference between the current value and a known current value, then dividing the difference by a constant.

36. The method of claim 35, wherein the known current value, the know temperature and the constant are stored in a memory.